Ground Bounce Spec Sheet

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1 PCB Overview

THE aim of this PCB is to observe the undesirable characteristics of discrete IC packages—namely, the ground bounce induced by the package's ground lead inductance.

We drew inspiration from the circuit on p. 71 from [1]. The idea is we charge 3 flip-flops in the same package to VDD, then discharge them so that there is a high change in return current going through the ground pin. Due to the ground lead's non-zero inductance, this current change introduces a voltage difference between the package's "ground" and the ground of the PCB. This is what ground bounce.

The ground bounce can be observed by "looking" into the package ground with respect to the PCB's ground through the output of a grounded input flip-flop. A 1kΩ series resistor is used as a terminator to match any input impedance when measuring the ground bounce.

2 Component List and Specifications

- Integrated Circuits (ICs)
  - U1 : LM7805 (Voltage Regulator, TO-220)
  - U2 : CD74HCT174 (Hex. DFF, DIP)
  - U3 : SN74LS05 (Hex. Inverter, DIP)
- Connectors
  - J1 : SMA Board Connector
  - J2 : 2-pin standard header
  - J3 : 2-pin standard header
- Diodes
  - D1 : 1N4001 (TO)
- Resistors
  - R1 : 1kΩ (0805)
- Capactitors
  - C1 : 10pF (0805)
  - C2 : 10pF (0805)
  - C3 : 10pF (0805)
  - C4 : 100nF (0805)
  - C5 : 100nF (0805)
  - C6 : 100nF (0805)
  - C7 : 100nF (0805)

3 Electrical Specifications

Both the U2 and U3 need a nominal supply voltage of 5V. U1 is a voltage regulator with an output voltage of 5V. Perfect. U1 can takes a nominal input voltage of 10V, with an acceptable range between 7.5V and 35V. 35V is the absolute maximum according to its spec.

U1's datasheet also recommends an inline diode to protect the external power supply. This is D1's purpose. Additionally, filtering capacitors at the input and output are recommended, being 220nF and 100nF, respectively.

100nF filtering capacitors across the supply pins of U2 and U3 are also good practice so we get clean power delivered to these components.

The clock signal connected to the system should be 100kHz, 5Vpp, and offset +5V.

4 Schematic, PCB Layout, Notes on Novel Features

4.1 Schematic

Our schematic entry from Altuim is found in Figure 1. The setup for the hex. DFF is very reminiscent of the one found in [1]. The hex inverter is essentially delaying and inverting the clock signal to pull down the signals to ground after fully charging from the previous clock rise.

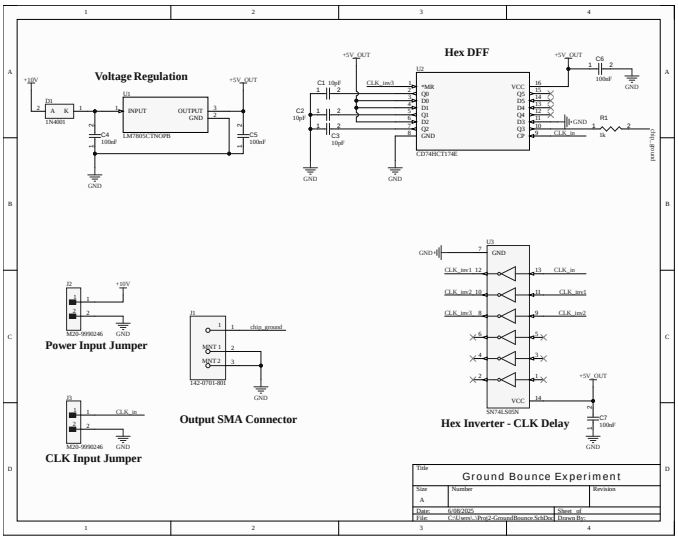

Figure 1: Schematic entry of our ground bounce circuit.

here would be the signal we're reading after R1, but the purpose of R1 is to stop any reflections we'd get from impedance mismatches.

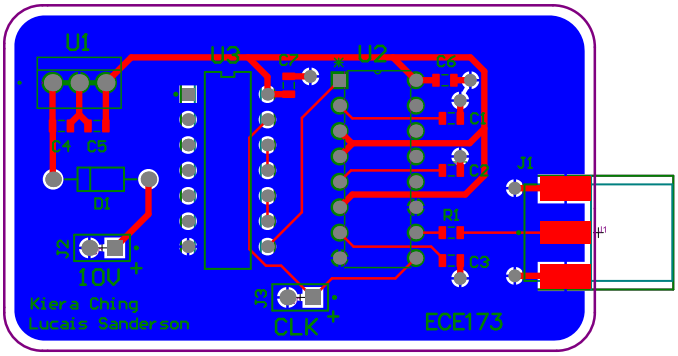

Figure 2: 2D view of our PCB design.

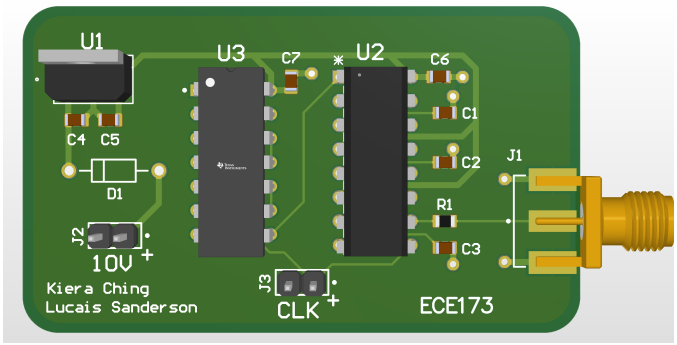

Figure 3: 3D rendering of the top of our PCB design.

4.2 PCB Layout

Our primary goal with the layout was to maximize area utilization while remaining practical to hand-solder because some components are THT.

U1 needs its filtering caps to be as close as possible to its pins. They could be close than shown in Figures 2, 3. This is the same as the filtering caps for U2 and U3.

We ran power traces with 25 mil widths, giving plenty of room for our current needs. A ground plane was employed on the bottom side, so all return paths that we aren't interested in shouldn't be an issue.

All signal traces are 10 mil. Impedance matching isn't really an issue on our operating speed (100kHz), so we just needed traces able to carry the current we need. The only concern

4.3 Novel Features

Our design is undeniably similar to that found in [1]. However, how we implemented the delayed reset might be novel. Instead of using something like an RC circuit to control the reset signal, we analyzed the datasheets for U2 and U3. The inverters in U3 have a finite rise delay. This delay lies between 9ns and 19ns. We are also given the DFF's clock to Q and rise times, which we can use to find how many inverters we need so that the DFFs can charge fully before being reset.

The total delay we want from the inverters is at least $t_{C2Q} + (t_{TLH}/2) \approx 20$ ns from U2's data

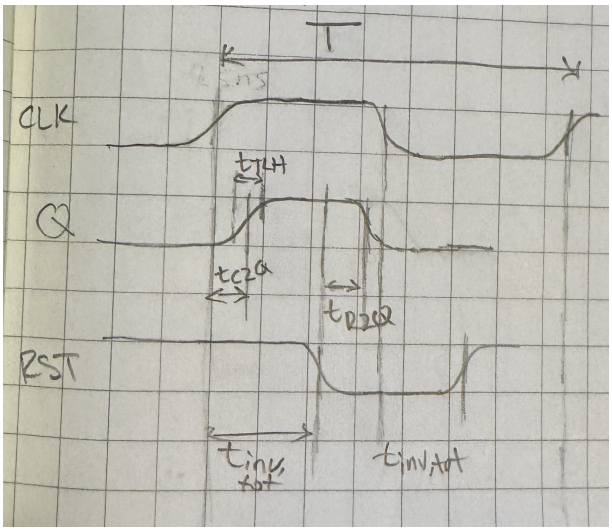

Figure 4: Timing analysis using inverters as buffers for delay.

sheet. Given this, 3 inverters at 9 ns delays give us a 27 ns delay, more than enough time for the outputs to charge. The timing analysis can be seen in Figure 4.

5 Theory & Expected Output

The idea of this experiment is that every signal needs a return path. Conservation of energy, even wave energy, and all that. So, take a signal line in Figure 5.

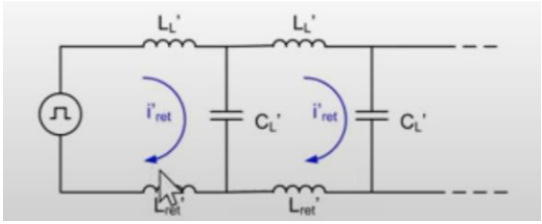

Figure 5: Circuit showing the inductance experienced by the signal at the wire bond/lead of a package. Image from Jason's slides.

Due to this, when viewing the voltage at the node between C'_L and L'_{ret} with respect to the ground of the signal, we would expect the transient response of an inductor after introducing a sharp change in current. It would look something like the graphic in Figure 6

Simple observation of the ground bounce effect is nice, but we want to solidify this

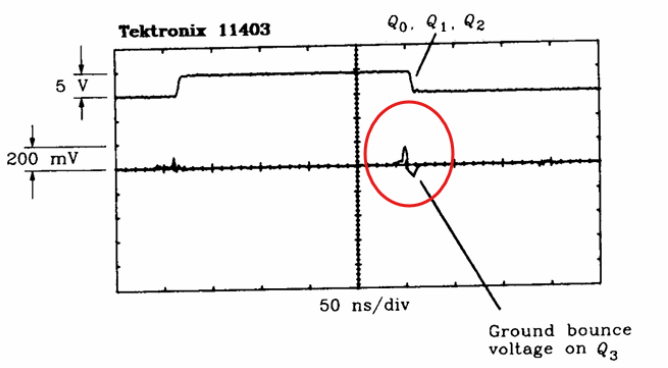

Figure 6: Graphic from an oscilloscope showing the effect of ground bounce. Reprinted from [1].

concept with numbers! We should be able to estimate the lead inductance of the IC's ground pin using the formula for ground bounce found in [1]:

$$\left|V_{GND}\right| = \left(L\frac{1.52 \cdot \Delta V}{T_{10-90}^2}C\right) \cdot \#signals \quad (1)$$

This equation implies we use a capacitive load, which we are. We can use some rough numbers for these variables. $\Delta V_{Max} = 5V$, $T_{10-90} = 4.7$ ns for this logic family, $C = 10$ pF, and 3 signals. Given these assumptions, a simple relation for L is

$$L = \frac{|V_{GND}|}{1032142.4} \quad (2)$$

So, when we measure the V_{GND} then we can estimate the lead inductance. Via [1], the lead inductance of a 14-pin plastic DIP (matching our DFF IC) should be about 8 nH.

6 How-To

You'll need:

- A power supply capable of 10V output
- A function generator or something that can produce a 5V, 100kHz clock signal
- 50Ω TV cable and a SMA/TV adapter
- Oscilloscope
- Test board populated with components

With your equipment turned off, clip on the 10V power to the corresponding headers (J2) denoted by the legend. Do the same with the

clock signal (J3). Hook up the oscilloscope to the SMA output (J1).

Now, turn on your power supply for 10V. Turn on your clock signal. Turn on your scope and observe. You should see ground bounce now!

7 Testing, Validation, and Troubleshooting

Our group didn't receive our board in time so we'll be covering the testing we did with a breadboard prototype.

We started with 3 10 pF load capacitors, as shown in Figure 7. This is our breadboard prototype circuit.

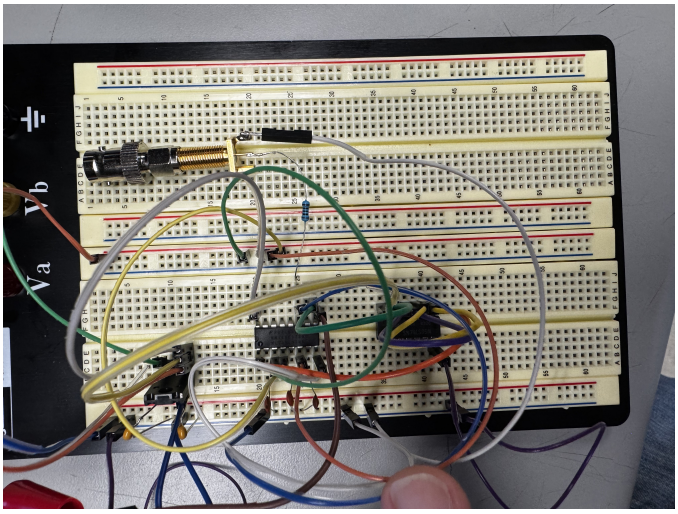

Figure 7: Picture of our ground bounce breadboard prototype.

The results using all same load capacitance values of 10 pF yielded the waveform in Figure 8. Not very helpful... And this doesn't look much like what we expected from Figure 6. Instead, we're seeing a lot of ringing, seeming reflections; generally unintelligible information. Our thinking is that using identical capacitors led to synchronization (same RC delays), in turn leading to constructive interference. Suffice to say, we decided to try different load capacitance (credit to Mishari for this suggestion).

After swapping the load capacitors for different values, namely $C_1 = 10$ pF, $C_2 = 15$ pF, and $C_3 = 22$ pF, we saw the waveform in Figure 9. This waveform is much cleaner and is more

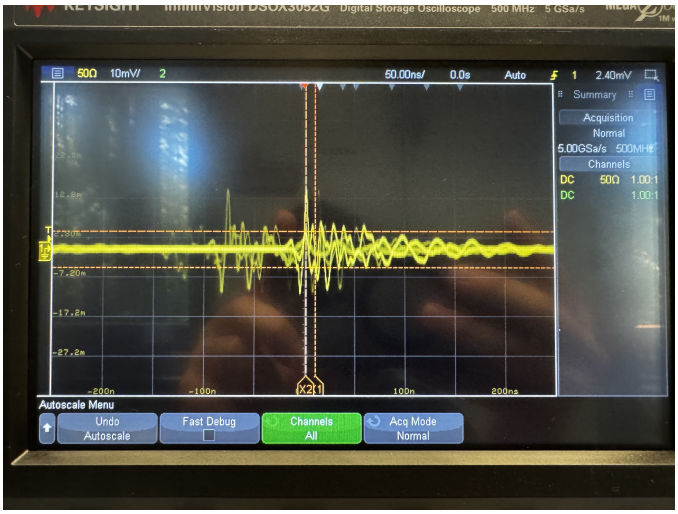

Figure 8: Resulting waveform using $C_1 = C_2 = C_3 = 10$ pF.

reminiscent of that in [1]. However, because we have 3 different valued loads, we are getting 3 staggered instances of what we expect to be ground bounce. This makes sense as 3 different loads leads to 3 different RC circuits of varying amplitude. The delay can be *roughly* broken down to $D = 0.69RC \rightarrow D \sim C$. So we can assume the leftmost "dip" and "peak" is that of the 10 pF capacitor, the second dip-peak as the 15 pF, and the third as the 22 pF.

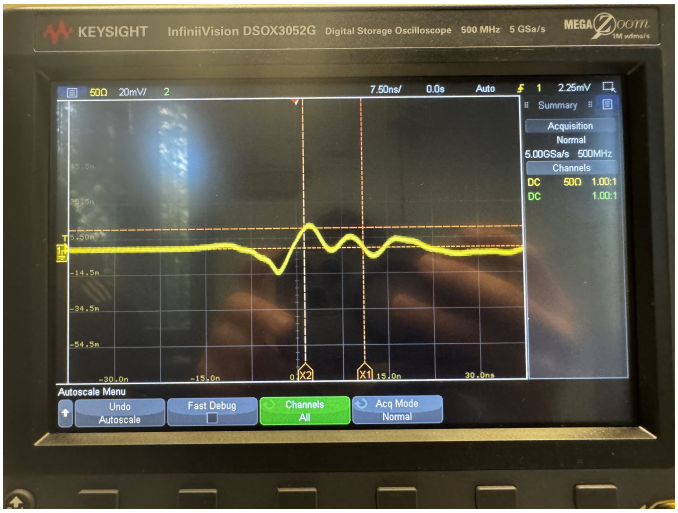

Figure 9: Resulting waveform using $C_1 = 10$ pF, $C_2 = 15$ pF, $C_3 = 22$ pF.

So, after some troubleshooting, we got the waveform that we desired. We were able to control this perceived ground bounce by changing

the load capacitances which the formula we discussed in the previous section predicted. I call this a win, though we will only know for sure if our lead inductance from this waveform's magnitude is close to that magic 8 nH.

8 Question and Answer

8.1 Estimate what the actual bondout inductance is and compare it with published data.

The waveform from Figure 8 is not clean enough to get a reliable reading. So we have to look to Figure 9. But this changes our expected lead inductance from earlier, right? Because that expression was obtained assuming identical capacitances. Instead, we'll take the magnitude of the first dip-peak from Figure 9 and run with that. The magnitude there is ~ 29 mV. Recalculating L for just one signal,

$$L = \frac{|V_{GND}|}{3440470.8} = 8.428 \times 10^{-9} H \tag{3}$$

Look at that. Our result from our prototype yielded an inductance of 8.428 nH. This is a 5.2% difference from our expected 8 nH.

8.2 Determine what the fastest edge times need to be before signal integrity is compromised for the logic family chosen for your experiment, and discuss how this related to actual circuits employing devices from this same logic family.

For the 74HCT logic family (via the datasheet), the low voltage level is read below 0.8V. When ground bounce introduces a voltage difference above this, we'll consider the signal integrity compromised. Given this, let's also assume we have a single 10 pF load on one of these DFFs. So,

$$\left|V_{GND}(T_{10-90})\right| = (8[nH])\frac{1.52 \cdot 5[V]}{T_{10-90}^2}10[pF] \tag{4}$$

$$= \frac{6.08 \times 10^{-19}}{T_{10-90}^2} \tag{5}$$

Now, we'll let $V_{GND} = 0.8$V.

$$0.8 = \frac{6.08 \times 10^{-19}}{T_{10-90}^2} \tag{6}$$

$$\implies T_{10-90} = \frac{6.08 \times 10^{-19}}{0.8} = 3.8 \times 10^{-19}[s] \tag{7}$$

That is 38 aS (attoseconds). *Very* short.

8.3 There are other bondout inductances besides that connected to the common ground pin. Discuss whether and when these other inductances should be considered.

The other boundout inductances aren't as important as the one associated with the ground pin. This is because voltages seen at signal pins are meant to change. We assume that "ground" is a static reference W.R.T. every other voltage.

8.4 Many mixed-signal chips have separate pins for analog and digital grounds, as well as for power pins.Discuss why this is done and comment on how the ground bounce phenomemon within a digital chip applies to how power and ground are routed in pcb designs having multiple devices.

The reason separate digital and analog ground pins are use is because the analog part of the system could be returning some very high frequency signals through the ground pin. If the same ground pin was used, then these high frequencies could induce a voltage on the ground pin (due to its lead inductance), temporarily making our perfect ground reference not perfect. In effect, this voltage could mar the signal integrity for our digital system.

8.5 Some digital only devices have multiple power and ground pins. Discuss whether there can be any advantage to this practice.

There could definitely be an advantage to this. The signals will attempt to take the shortest path back to its source, so if there's a route through a different pin that's closer then it'll take that. This is good in the case that multiple signals are switching simultaneously (as was in this experiment). In effect, the current load

is distributed and we aren't trying to squeeze all of the current through one pin. Thus, the induced voltage is less per pin.

9 Conclusion

Overall, I'd say our experiment was a success. Admittedly, our design isn't very novel, maybe apart from how we achieved our delayed reset. Additionally, we didn't get to test our actual PCB due to time constraints. But, our crude breadboard prototype worked after some troubleshooting and we, seemingly, got a pretty close approximation of a known value from our results.

10 Group Contribution Statement

The first schematic design was done by me. I looked into all of the datasheets to figure out how many inverters we needed and to make sure our clock rate was slow enough to allow everything to operate.

After discussing some of the design with Kiera, like honing in on which type of components we need and confirming the timing, she entered the schematic and sourced the footprints we needed.

When we wanted to test that our tentative design at least functioned, we built a breadboard prototype. I soldered the SMA connector to the resistor and wire for ground. Kiera assembled the circuit and we collectively troubleshooted why the signal looked like it did.

I did most of the placement and routing for the layout phase, consulting Kiera on some design choices such as whether to include a ground plane or not, etc. I also validated the manufacturability by using AdvancedPCB's service.

Overall, I think the workload was pretty balanced and we collaborated very well.

Acknowledgments

References

[1] H. W. Johnson and M. Graham, High speed digital design: a handbook of black magic, 30. pr. Upper Saddle River, NJ: Prentice Hall PTR, 1993.