Lucais Sanderson

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Education

B.S. in Computer Engineering, emphasis in Digital Hardware **June 2025**
Minor in Electrical Engineering
Minor in Computer Science
University of California, Santa Cruz GPA: 3.67/4.0

Relevant Coursework: Computer Architecture, Digital/FPGA Design, Logic Design, Circuit Analysis & Design, VLSI, Embedded System Design, Digital Signal Processing, Data Structure and Algorithms, Signals and Systems, Analog Electronics, Embedded System Design, and High-Speed Digital Design

Projects

AM/FM Radio Receiver PCB (Independent) **July 2025**
Analog + Digital PCB Design

- Designed a 2-layer AM/FM radio PCB (Si4825 + PAM8302) with analog filtering, decoupling, and power routing.
- Built schematics and layout in Altium; followed RF layout practices for audio and antenna signal integrity.

VLSI CPU Core PPA Optimization **March 2025**
Advanced VLSI

- Optimized Ibex RISC-V core using OpenROAD/OpenLane2 with custom memory macros and manual floorplanning.
- Reduced area by 42.5% (2.71 mm^2 → 1.56 mm^2) and nearly doubled frequency (10 MHz → 19.2 MHz).
- Performed PPA tradeoff analysis, congestion debugging, and timing closure across process corners.

IoT Sensor Network and Web Dashboard **June 2025**
Internet of Things

- Built a fully decentralized sensor network with Raspberry Pis using tree and token ring topologies to autonomously relay environmental data.
- Architected a robust aggregation system and dynamic sink node to route data into a custom web server using Flask and MySQL.
- Developed a slick, interactive full-stack dashboard (HTML/CSS/JS + XAMPP) to visualize real-time telemetry with automated updates.

Ground Bounce Analysis PCB **June 2025**
High-Speed Digital Design

- Designed and fabricated a custom 2-layer PCB to provoke and quantify ground bounce on a hex DFF using precision-timed inverter delays.
- Integrated clean power delivery (LM7805), calculated decoupling, and tuned capacitive loads to simulate worst-case switching transients.
- Captured transient ground excursions with oscilloscope measurements and analytically estimated pin inductance for validation.

Chromatic Tuner on FPGA **December 2024**
Logic Design with Verilog

- Designed a fully functional pitch detection system in SystemVerilog, deployed to an iCEBreaker FPGA with modular architecture.
- Verified behavioral correctness through simulation (Verilator) and iterative debugging, from audio sampling to LED-based pitch display.

Morse Code Communication with LEDs **May 2024**
Embedded System Design

- Created a wireless light-based messaging system between Raspberry Pi and ESP32 using LED pulses and analog/digital interfacing.
- Implemented a reliable FSM decoder in ESP-IDF with RTOS scheduling and analog signal conditioning for robust message recovery.
- Achieved 220+ char/sec transfer rate with onboard real-time feedback and noise filtering logic.

Osmosis Game Design Project **December 2023**
Logic Design

- Designed a playable game using FSMs and VGA signal generation on a BASYS FPGA, synchronized with user inputs and visual events.
- Demonstrated precision timing logic, pixel control, and modular code structure in Verilog.

Flip Flop Design Project **December 2023**
Logic Design

- Constructed a custom negative-edge D flip-flop with active logic integration, verified using LED-based I/O and scope analysis.
- Delivered a refined test plan and tech documentation capturing setup, timing diagrams, and propagation edge behavior.

Big Integers ADT **May 2023**
Data Structures and Algorithms in C++

- Engineered a BigInteger arithmetic library for unbounded signed integers using dynamic linked-list storage.
- Enabled base conversion, carry logic, and signed operations with clean encapsulation and modular structure.

LZ77/78 Compression Algorithm **March 2023**
Computer Systems & C Programming

- Implemented sliding-window text compression based on LZ77/LZ78 principles, optimizing for memory footprint and redundancy.
- Documented algorithm structure and edge-case handling in clear technical prose, bridging implementation with theory.

Work Experience

Cashier / Sales Associate **June 2019 - October 2023**
Roaring Camp Railroads Santa Cruz, CA

- Served up to 500 customers per day during peak season, handling ticketing, refunds, and event sales with accuracy and clarity.

- Upsold premium offerings, guided guests through schedules, and resolved account issues with professionalism.
- Operated POS systems and maintained orderly front-of-house operations under pressure.

Field Technician, Irrigation Systems **August 2020 - January 2021**
Bamboo Giant Aptos, CA

- Supported large-scale irrigation installs, coordinating hardware layout and real-time system checks across multi-acre zones.
- Communicated system requirements and updates within the team to ensure project flow and customer satisfaction.

Skills

- **Programming Languages:** Verilog (2 years), SystemVerilog (<1 year), C/C++ (2 years), Python (4 years), RISC-V (2 years)
- **Tools:** EDA (Cadence), GitHub, Latex, Excel, Word, Photoshop, Illustrator
- **Operating Systems:** Linux (various distributions), UNIX/MACOS, Windows